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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/314,750	05/19/1999	HIROSHI MURAKAMI	0941.63081	5601

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GREER, BURNS & CRAIN
300 S WACKER DR
25TH FLOOR
CHICAGO, IL 60606

EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/314,750	MURAKAMI, HIROSHI	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

ETAILED ACTION

1. ***Response to Arguments***

1. In view of the Appeal Brief filed on April 13, 2005, PROSECUTION IS HEREBY REOPENED.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

The filed is entered.

2. Applicant's arguments with respect to claims 2-11 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Objections

4. Claim 2 is objected to because of the following informalities: information sorted in line 17 is supposed to be "information stored". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-11 are rejected under 35 U. S. C. 102 (e) as being unpatentable over U. S. Patent # 5,815,136 ("Ikeda et al.") in view of US Patent # 6,598,136 ('Norrod et al.').

As for claim 2, Ikeda et al. teach a display device (Fig.16 and 18A) comprising:

a display unit, which displays an image (liquid crystal display Fig.16 (132));

a display-data line, which supplies data of the image from an exterior of said display unit (data bus Fig.18a (102));

an operation circuit unit which controls said display unit to display the data of the image supplied through said display data line based on the information stored in said memories (liquid crystal driver Fig.18A (105-1));

a data bus (1605) which connects said memories to an exterior of said display device and supplies the information to said memories from the exterior of said display device; and

an address bus (1604) which connects said memories to the exterior of said display device, and supplies address signals for selecting one of said memories; a gate driver (scanning circuit Fig.16 (130) which drives the gate lines;

the data driver (drivers 105-1 and 105-2) which drives the data lines of said display unit, wherein at least one of said gate driver and said data driver operates based on the information stored on said memories.

The prior art teach all the claimed limitations with the exception of providing memories which store information for controlling displaying of the data of the image on said display unit said information being different from said data image.

However, Norrod et al. teach memories which store information for controlling displaying of the data of the image on said display unit said information being different from said data image (a CPU Fig.2 (10) which includes a plurality of memories like memory controller (28), L2 cache controller (24) and L1 cache (18) (scratchpad) (column 4, lines 57-64).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the memories in the CPU as taught by Norrod et al. in the liquid crystal display disclosed by Ikeda et al. because this would provide a programmable address register as part of the control circuitry in the scratchpad memory to control display (column 3, lines 9 and 10).

As for claim 3, Ikeda et al. teach a shift register Fig.2 (205-1) corresponding to the gate and data drivers include a shift register.

As for claim 4, Ikeda et al. teach a decoder Fig. 18A (118-2) corresponding

to the gate and data drivers include a decoder.

As for claim 5, Ikeda et al. teach a address counter Fig. 29A (155) corresponding to the gate and data drivers include an address counter.

As for claim 6, Ikeda et al. teach a memory controller 807 is connected to the address bus 804, the data bus 805 and the control signal bus 806 so that the CPU 801 can access each of the main memory 802 (column 27, lines 48-51).

As for claim 7, Ikeda et al. teach a memory controller 807 is connected to the address bus 804, the data bus 805 and the control signal bus 806 so that the CPU 801 can access each of the main memory 802 (column 27, lines 48-51).

As for claim 8, Ikeda et al. teach the address converter of each of said driver circuit elements converts the address given from said external device into an address of the display memory of that driver circuit element on the basis of said driver identification information indicative of that driver circuit element (column 42, lines 59-64) corresponding to a display-information acquisition circuit which acquires information about said display unit; the CPU Fig. 16 (1601) which may include a lot of memories which is different from the main memory Fig. 16 (1602) corresponding to display-information memories which store the information about said display unit.

As for claim 9, Ikeda et al. teach if the display operation is not performed at the fixed period, the quality of display of the liquid crystal panel is deteriorated. In the present embodiment, the two stages of latch circuits 187 and 189 are provided for enabling the display operation at the fixed period even in the case

where the updating access and the display access overlap (column 30, lines 26-32) corresponding to a display-information acquisition circuit checks said display unit to acquire information about said display unit with regard to a defect of said display unit.

As for claim 10, Ikeda et al. teach the address converter of each of said driver circuit elements converts the address given from said external device into an address of the display memory of that driver circuit element on the basis of said driver identification information indicative of that driver circuit element (column 42, lines 59-64) corresponding to said display data acquisition circuit acquires the information about the said display.

As for claim 11, Ikeda et al. teach the data lines 136 and the scanning lines 137 are arranged in a matrix form so that 320.times.240 pixels are formed at the intersections of the lines 136 and 137 (column 10, lines 6-8) corresponding to a plurality of pixel electrodes corresponding to the respective polysilicon thin film transistor. It is well know in the art to have a polysilicon thin film transistor.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park 11, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art unit 2674

Date 6/24/2005

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER